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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,647	09/30/2003	Kwang Su Choe	YOR920030293US1 (16818)	4796
7590 Steven Fischman, ESQ. Scully, Scott, Murphy and Presser 400 Garden City Plaza Garden City, NY 11530	06/14/2007		EXAMINER PADGETT, MARIANNE L	
			ART UNIT 1762	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/674,647	CHOE ET AL.
	Examiner	Art Unit
	Marianne L. Padgett	1762

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 6/30/2005 & 9/30/2006.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-25 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 6/30/5.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application
- 6) Other: _____.

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1. Claims 4-6, 8-12, 23 & 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

While claim 4 & its dependent claims 5-6 require that the providing step "comprises an electrolytic anodization process", nowhere in this set of three claims is there any limitation that states what is being anodized, i.e. there is no positive requirement as to what these process steps are applied to, and while one might guess that it is the "structure" as a whole, or the structures "Si-containing substrate", or some other unspecified portion of the substrate, a guess or an assumption is **not** a proper or clear or positive patent limitation, hence the meaning of these claims lack definiteness.

In claim 8, while the claim provides limitations concerning **what** is formed ("a single crystal Si-containing layer) & **when** it is formed (between providing & implanting steps), there is no requirement or positive statement as to **what** is formed. In other words while the examiner might guess or assumed that applicant intended for this layer to be deposited on the substrate, there is no necessity in the claims that it is even deposited in the same chamber, same room, same continent, only that it is deposited at the time it is between providing a substrate/structure (i.e. finding or deciding on a substrate) & implanting the structure with oxygen ions.

Claim 8 is further unclear, as it is uncertain what is meant by "a single crystal Si-containing layer", especially when considered in light of claim 9 which depends therefrom. What is unclear is whether the layer itself is entirely made up of a single crystal, where that single crystal layer is Si-containing, which would be logical considering the normal meaning of single crystal requiring their to be only one crystal, however claim 9 contradicts this potential logical meaning by requiring the layer to contain things they can't possibly be part of a single crystal, such as amorphous or polycrystalline silicon! Does this combination of limitations indicate that applicants consider each crystal grain in a polycrystalline layer to be a single crystal? This would be a logical conclusion of applicants' structure of

claim limitations, but it is highly inconsistent with the meaning of standard nomenclature for single crystal & polycrystalline materials. For these reasons, the intended scope & means of the limitations of claims 8-9 are indeterminable, and any possible meaning will be considered to apply to either claim, i.e. the layer may be a single crystalline material that contains Si, single crystal Si, epitaxial Si (whether or not it fits the standard definition of single crystalline), amorphous Si (has no crystals whatsoever), SiGe (any crystalline or amorphous microstructure), polycrystalline Si, or any mixtures of these materials.

Note as claims 23 & 25, contained the phrase "a single crystal Si-containing layer", which is seen above to have unclear meaning in the claims as written, the meaning in these claims is also unclear.

Following the same pattern of a lack of context, claims 10-11 while claiming **when** a "bake step" occurs, do not apply it to anything in particular, nor is this bake step required to have any particular effect on the unknown to which it is applied. These claims lack a positive or meaningful connection to the process of the independent claim.

In claim 12, it is uncertain whether "an ion dose from about 1E16 to 1E17 atom/cm²" is further defining the "an oxygen dose..." previously introduced in independent claim 1, or if it is introducing a new ion dose of some other unspecified ion, since the new term in claim 12 uses inconsistent terminology with respect claim 1 & doesn't use an article that shows antecedent basis. For purposes of considering art, either option will be considered to read on this claim due to the above ambiguities.

2. Applicants' IDS of 6/30/2005 is made of record, where it is noted that the PCT reference cited is the child of this case, & the Japanese patent JP9-64323 provided was cited in the PCT search report along with its JPO abstract & rated X for claims 1-9, 12-15 & 18-23, plus Y for 6, 11-17 & 19, but only the Japanese document was founded and scanned file (i.e. no the Patent Abstracts of Japan (i.e. English abstract) referred to in the search report is present), however the examiner has found and provided two different copies of machine translation is & the JPO English abstract. The PCT search

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report referred to a literature document to Chen et al. as rated Y for claims 13, 16-17 & 19, which was also not provided to the PTO, nor cited on the PTO-1449.

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-6, 8-9, 14-16 & 21 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ikeda Tadashi (JP 09-064323; also see Patent Abstracts of Japan & 2 machine translations).

First, it is noted then in applicants' specification in paragraph [0026], they redefined the phrase "Si-containing", which has a plain meaning of anything containing silicon, to have the narrower meaning of "a semiconductor material that includes at least silicon".

Ikeda teaches employing a semiconductor substrate, that may be a silicon wafer, which has been doped to be either n-type or p-type, and treating it with a HF solution, with an exemplary current density of 10-80 mA/cm² creating a porous silicon layer of a desired thickness (~ 100 nm exemplified) via anodization (figures 1 (a-b) & 2 (a-b); [0015-16]; [0022] & [0027]). Thereafter, a single crystal silicon layer is deposited over the porous silicon layer, then oxygen ions are implanted through the single crystal silicon layer into the porous silicon layer, after which the treatment is performed at temperatures of 1200-1350°C, so as to form an "embedded oxide film layer" from the ion implanted porous layer, which due to the overall oxidation processing technique is taught to not increase in volume from that of the original porous layer. Options of uniformly ion implanting or using a patterned resist to mask areas during ion implanting, with potentially multiple ion implantings are taught (figures 1 (c-e) & 2 (c-e); [0017-19] & [0022-25]). Ikeda notes that their techniques solves problems discussed with respect to the conventional processes illustrated in figures 3 & 4.

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5. Claim 7 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ikeda Tadashi.

Claims 12-13, 18-20 & 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda Tadashi.

While Ikeda teaches creating a porous layer (\equiv porous Si-containing region), the percentage of that layer which is porous is not disclosed, however at the claimed range of "about 0.01 % or greater" is so broad that it covers virtually any conceivable amount that may be produced by Ikeda's process & still be called porous. Furthermore, the anodization technique used by Ikeda to create the porosity is essentially the same as the anodization process claimed by applicants & discussed in applicants' specification on [0029-32] as used to convert doped a single crystal silicon to porous silicon, thus like porosities would have been expected to have inherently been produced from like processes & materials. Alternately, it would've been obvious to one of ordinary skill in the art to create sufficient porosity in order to effect Ikeda's taught process of creating an embedded or buried oxide layer, where volume increase is not a problem (i.e. avoid crystal & stress defects caused by increased volume during oxidation), such that the compositional parameters, such as degree of doping & the HF anodization parameters would have been optimized based on those taught in order to produce required porosity for required effects.

Ikeda does not teach that the claimed ion dose of "from about 1E16 to about 1E17 atoms/cm²", however they do teach optimizing the volume ratio between the Si:O to about 1:2, and that in their particular example the amount of oxygen implanted was about 10¹⁸. It would've been obvious to one of ordinary skill in the art to optimize the dosage applied over the area being ion implanted dependent on the density of the porous area (i.e. more dense has more silicon, while less dense has less silicon, thus directly affecting the amount of oxygen needed to effect the ratio of Si:O) & the thickness of the buried oxide layer being for, as the thickness will also affect the amount of oxygen required to create the desired ratio

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for effective oxide formation in the oxygen ion implanted porous layer. Other ion implantation parameters, such as beam current, energy & temperature, are not discussed by Ikeda, however it would've been obvious to one of ordinary skill in the art to determine via routine experimentation such useful parameters for affecting the taught ion implantation, as they would be required to be determined in order to perform the taught process, where analogous parameters would have been expected, since analogous effects are being produced in like materials with like ions & analogous or overlapping structural results.

While Ikeda teaches the heat treatment employing claim temperatures of 1200-1350°C, Ikeda does not discuss the atmosphere under which this heat treatment to create the embedded oxide layer is performed, however it would've been obvious to one of ordinary skill in the art that as one is creating an oxide to employ atmospheres that have an oxygen ambient using a common source of oxygen, such as those claimed, where the atmosphere is otherwise unreactive or has no reaction that interferes with oxide formation (which would suggest to one of ordinary skill in the art use of inert gases to achieve desired pressure, prevent contamination, or like standard purposes), since such would have been expected to prevent out-gassing of oxygen, which could decrease the desired stoichiometry, & since performing oxidations under oxygen atmospheres is a standard procedure. It is noted that use of such an oxygen containing atmosphere during the heat treatment process/annealing would inherently affect the surface of the single crystal silicon layer to affect thermal oxidation thereon, and as such would be further desirable for particular device formation sequences which require such a surface oxide layer.

6. Claims 1-15 & 18-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Houston et al. (2002/0086463 A1).

Houston et al. teach making an silicon-on-insulator (SOI) wafer, where a first layer of porous silicon is formed by anodizing a boron (i.e., p-type) doped silicon wafer using a HF solution, such that the depth of the porous silicon is controlled by the timing of the anodization treatment or by limiting the depth of the boron doping, where thicknesses in the range of nanometers to microns can be obtained

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([0006]; [0016]). Houston et al. teach that the anodizing process can result in cracks on the surface of the porous silicon, hence they employ a "prebake" process that fills up surface pores with migrated silicon atoms in order to reduce the surface energy. This "prebake" process seals the surface; may employ a hydrogen ambient; and the sealed surface may provide a starting point for subsequent epitaxial growth of a layer on the surface, where the quality of the epitaxial layer may depend on the surface pore filling during the sealing bake ([0006]; [0018-19]; [0022]). The epitaxial semiconductor layer may be deposited on the sealed surface either before or after oxygen ion implanting, where the ion implanting may be carried out via plasma oxygen implant or other oxygen implanting methods, with the oxidizing species derived from molecular oxygen or other sources, such as ozone or N₂O, and where oxygen doses may be on the order of 10¹⁷-10¹⁸ oxygen ions per cm², which overlaps with claimed dosages ([0006]; [0016]; [0020]; 0023-25] & [0031]). The oxidation process, which forms the buried oxide layer from the implanted oxygen is completed by high-temperature anneal, which appears to use temperatures on the order of 1000°C for about 30 minutes ([0006] & [0020]). Houston et al. teach their process provides a number of advantages ([0007-11]), inclusive of aiding a planarity, sharp definition of the oxide layer, etc.

The teachings of Houston et al. differ from the present claims by not providing a specific thickness for the porous layer or the resultant buried oxide layer produced by its oxygen implantation & anneal, however as Houston et al. teach means for controlling the thickness of the porous layer, hence the buried oxide layer, suggesting its thickness measurements can be in the range of nanometers, it would have been obvious to one of ordinary skill in the art that contemplated thicknesses for the buried oxide layer include thicknesses as claimed of about 100 nm or less, as the teachings of nanometer range is suggestive thereof & as the intended use relates to integrated circuit structures where such thicknesses would have been considered typical for typical desired miniaturization of circuit designs.

Houston et al. did not provide claimed parameters for current densities for the anodization process nor for the ion implantation process, nor ion beam energy as for implantation, nor temperatures

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for baking to seal the porous surface in the hydrogen ambient, however given the taught process of Houston et al., one of ordinary skill in the art would have been expected to employ routine experimentation to determine necessary parameters not explicitly given, such as current densities, energies & temperatures, in order to employ the taught procedure to produce the taught results, which would have been expected to be inclusive of claimed ranges, as no critical differences seen in their effects from those claim. Note that Houston et al.'s teaching of the implanting oxygen with plasma or other ion implantation methods, would have been suggestive to one of ordinary skill in the art of oxygen plasmas or oxygen ion beams to effect the oxygen implantation, where the parameters of either technique would have been optimized to produce doses on the order claim, noting that in paragraph [0006] Houston et al. teach implantation of low oxygen doses, and that the 10^{18} O ions/cm² is considered to be a relatively heavy dose [0020], which teachings would suggest to one of ordinary skill an apparent preference for the lower end of the taught dosage range.

It is noted that while Houston et al. has much discussion on growing of an epitaxial layer (epi layer), its material is generally not identified, although [0023 & 25] refers to it as an epitaxial semiconductor layer, but [0024] in the same sequence only refers to a semiconductor layer, not mentioning epitaxial, while [0006] also does not discuss an epitaxial layer in the process sequence, instead discusses forming a thin silicon film by standard deposition techniques on the sealed porous silicon layer, hence growth of an epitaxial silicon layer on the sealed H-prebaked surface is considered taught or suggested by Houston et al., or alternatively obvious due to the overlapping of the teachings for the desired deposit on the sealed surface as presented above.

7. Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Bendernagel et al. (6,800,518 B2, which incorporates PN 5,930,643 to Sadana et al. by reference).

The applied reference has a common assignee & overlapping, but not identical inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior

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art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Bendernagel et al. teach forming composite structures, which may include buried insulators (oxides), buried conductive & buried void plane structures, by forming a layer of porous silicon (or alternately forming vacancies or voids) in the surface region of a semiconductor substrate, such as silicon via electrolytic anodization with a HF-containing solution, where the porosity produced is mainly dependent on the current (~0.1-20 mA/cm²) & voltage (~0.1-10 volts typical, ~0.5-5 volts preferred) used, the HF concentration, and the dopant type & concentration in the wafer, and where thickness of the porous silicon layer may additionally depend on the time (~30 sec.-10 min., ~1-5 min. more highly preferred) of anodization process. For this process Bendernagel et al. teach that the "semiconductor wafer needs to be doped, preferably but not necessarily with p-type doping atoms. When a boron-doped p-type wafer is employed, the dopant concentration of the wafer is typically from about 1E15 to about 1E19 atom/cm³..." (emphasis added, col. 6, lines 18-26). Next it is taught that a brief anneal in hydrogen ambient at elevated temperatures may be employed to eliminate open pores on the surface of the porous silicon layer, thereafter an epitaxial silicon (epi-Si) layer on the surface, then the composite substrate is ion implanted, where the ions employed may be oxygen ions, when a buried oxide is intended, or optionally may include nitrogen ions, or just nitrogen ions for an alternate buried insulator, or metal ions for a buried conductor or void planes. Masking may optionally be employed, with a HF-resistant material (photoresist) before the anodization step &/or a patterned mask for selective ion implantation before implanting, which masks are removed before deposition of the epi-Si or after ion implanting, respectively. Oxygen ion implanting may be in a single or multiple steps, continuous or pulsed, or combined with other ion implantation steps depending on desired structure. Oxygen implanting

is taught to be via any conventional ion implantation apparatus, with any conventional ion implanting conditions employed, which are exemplified as O-ion dose from about 1E16-2E18 atoms/cm², implantation energy from about 50 KeV-10 MeV, ion beam current density from about 0.05-500mA/cm², and ion implantation temperature from about 480-650°C. More preferred oxygen ion implantation conditions are also given (~5E16-2E17 atoms/cm², ~150-300 KeV, ~1.0-10 mA/cm², ~550-600°C) as well as this high-temperature ion implantation step followed by a normal room temperature ion implantation step exemplified in prior art references. After the ion implanting step(s) high-temperature annealing is performed to transform the implanted oxygen regions into buried oxide regions, while regions that do not contain oxygen ions can be transformed into buried void layers or buried conductive regions. The high-temperature annealing is performed at temperatures of about 1300°C or greater, but less than the melting point of Si, which is 1415°C, and may be carried out in atmospheres of pure oxygen (O₂), oxygen mixed with an inert gas or N₂, or either without oxygen, or vacuum. When annealing causes significant diffusion of dopants into the overlying silicon layer, a post hydrogen annealing process, which may use the same or different conditions (0.25-3 hours, ≤ 82 Torr H-ambient, T = 1100-1150°C) is then employed. Col. 9, lines 7-12 note that during annealing the porous silicon is consumed by the formation of the buried oxide/void, and that the epi-Si layer may be thinned by surface oxidation.

Bender Nagel et al. teach that the thickness of various layers of the composite structure may vary depending on process conditions employed during fabrication, where typically the buried insulating region has a more highly preferred thickness from about 5-200 nm, and that the thickness of the buried insulating regions is dependent on device requirement and could be controlled by adjusting vertical depth of the porous silicon layer formed during HF-anodization and the dose of the implanted ions. Particularly see the abstract; col. 2, lines 58-68; col. 3, lines 20-30 & 40-col. 4, line 44; col. 5, lines 10-15 & 27-39; col. 6, lines 17-col. 10, line 40, especially col. 6, lines 17-col. 7, lines 84 doping & anodization, col. 7, lines 9-31 for H-anneal to eliminate open surface pores, col. 7, lines 32-44 for the epi-Si layer, typically

monocrystalline structure ≡ single crystal, col. 7, lines 45-67 for masking, col. 8 for ion implanting & col. 9 for annealing.

With respect to applicant's claim 17, which is directed to specific parameters for a second oxygen implantation step, it is noted that Bendernagel et al.'s teachings on col. 8, lines 15-31 can be said to overlap with these parameters for their taught second implantation step at a normal room temperature, which is in the claimed temperature range for the second oxygen implantation, assuming that the other parameters employed for the second implantation can be any of the preceding taught parameters, which are overlapping with those claimed, or as suggested one may look at the exemplary art, such as USPN 5,930,643 by Sadana et al., which was **incorporated-by-reference**, that teaches forming buried oxide layers by creating a damaged buried region in a semiconductor substrate (Si) via oxygen ion implantation, possibly through a capping layer, using a low-dose ion implantation ($\sim\geq 5E16$) at high temperatures about $\geq 200^{\circ}\text{C}$, plus a second yet lower ion dose implantation at same or different energies carried out at cryogenic temperatures to about 300°C at doses of about $2E14-4E15 \text{ ion/cm}^2$. The ion implantation in Sadana et al. is followed by an oxidation step typically carried out in an inert ambient (N_2 or Ar) mixed with oxygen at temperatures from about 1300°C or higher, with optional further annealing of the oxidized structure (col. 2, lines 10-43), thus providing specific parameters for the two-step oxygen ion implantation alternative, which read on claim parameters and which are employed with oxidation & annealing procedures as taught and claimed.

8. Claims 1-25 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 14-38 of U.S. Patent No. 6,800,518 B2 (Bendernagel et al.), optionally in view of Sadana et al. (5,930,643).

Although the conflicting claims are not identical, they are not patentably distinct from each other because the Bendernagel et al. claims are directed to the same basic step with overlapping limitations with

respect to details, such as parameters, patterning or lack thereof (note that one may selectively implant an area predetermined to be the entire surface, i.e. blanket implantation), order in which specific limitations are emphasized, all of which may be considered obvious variations on the same theme. For instance, the patent to Bendernagel et al. claims forming a porous silicon layer in a surface region using parameters that overlap with claim parameters, thus while the specific porosity range of claims 7 is not claimed patent, due to the almost all-encompassing breath of about 0.1 % or greater porosity & the overlapping electrolytic anodization parameters, they presently claimed porosity range would have been expected to significantly overlap with expected effects of the patented procedure.

With respect to dependent claims 2-3, which require a silicon-containing (i.e. as defined on p.6, [0026] "a semiconductor material that includes at least silicon") substrate, which is doped (n-type or p-type) dopant, the claims in the Bendernagel et al. patent do not mention whether the semiconductor (Si) substrate is doped, however read in light of Bendernagel et al.'s specification, the substrate must be doped in order to perform the claimed electrolytic anodization (col. 6, lines 18-26 & 45-52; col. 7, lines 1-8; & col. 9, lines 41-45), thus n-type or p-type doping is considered to be compassed.

The patent claims also are not directed to a specific range of buried oxide thicknesses (about 100 nm or less), however as they are directed to a composite semiconductor structure expected to be used for finely patterned devices, one of ordinary skill in the art would have expected to produce layer thicknesses typical undesirable for such semiconductor devices which would have been expected to be inclusive of the range claimed, especially given a lack of significantly different critical procedures.

While the patent claims include oxygen ion implantation parameters of dose, implantation energy & ion beam current, as well as repeating the step of oxygen ion implant any number of times which overlaps with presently claimed oxygen ion implantation, including two oxygen implantation steps; the patented claims are not directed to the specific parameter of temperature during single or multiple oxygen ion implantations, however it would have been obvious to one of ordinary skill in the art to employ

conventional temperatures for ion being implantation, which would have been expected to encompass claimed temperature ranges, where choice of temperature would have been expected to be dependent on particular desired structure formation consistent with production of the claimed varied layers, thus expected to encompass claimed temperatures & employ different temperatures when the effects of the two steps are intended to be differentiated, as temperature is old and well known to affect resultant microstructure. Optionally, claimed temperatures for two oxygen ion implantations would have been further obvious in view of Sadana et al. (discussed above in section 7), who is also directed to creating buried oxide regions in semiconductors via oxygen ion implantation, where the desirability of providing two different effects (buried damage region & adjacent amorphous layer) via use of two ion implantations differentiated by dosage & temperature, is taught for controlling resultant oxide thickness & properties (col. 2, lines 1-43+; col. 4, lines 7-29 for first ion implantation & lines 30-65 for second ion implantation; col. 6, lines 8-16 note that the defect containing amorphous region is believed to enhance oxygen diffusion into the silicon & combine with the first created damage layer during the annealing step to form the buried oxide region; figure 2 & col. 6, lines 47-59 this 2-step 2 temperature ion implantation taught to improve electrical & structural qualities of oxide layer & save implant time & wafer cost), hence it would've been further obvious to one of ordinary skill in the art given the claimed parameters & claimed multiple ion implantations to employ a known technique as discussed in Sadana et al. for its taught advantages in producing analogous buried oxide layers using analogous ion implantation with analogous subsequent annealing techniques, with the expectation that advantages taught in Sadana et al. would also be relevant to Bendernagel et al.'s patented process. Also note that exemplary buried oxide region thicknesses via Sadana et al.'s process include 1000 Angstroms, i.e. 100 nm (example 1, specifically col. 7, lines 60-62), which provides further optional support for the above asserted obviousness of claimed thicknesses for buried oxide layers in semiconductor substrate constructions.

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9. Claims 1 & 12-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Sadana et al. (5,930,643), which was discussed above in sections 7 & 8.

As noted above, Sadana et al. (643) has all the parameters to the claimed oxygen ion implanting & annealing steps, for producing buried oxide layers of thicknesses claimed. While Sadana et al. does not discuss providing a silicon-containing semiconductor material in the substrate that has a region with "vacancies or voids located therein" the initial ion implanting step which creates defects with inherently include defects that may be described as "vacancies", as created date defects would have been expected to include displacements of atoms in the silicon-containing substrate, thus vacancies. Further note that while Sadana et al. most explicitly discuss a 2-step procedure, their teachings are inclusive of "this low temperature/low dose ion implantation step may be carried out in either a single step with a single temperature or multiple steps with multiple temperatures, which range from about cryogenic to about 300°C or less", such that the multistep ion implantation procedure described thereby reads on applicant's claimed process, even if one considers the "providing..." step necessarily separate from the step of "implanting...", as the multistep sequence to produce the low temperature low dose implantation, encompasses or overlaps with those sets of applicants' oxygen ion implantation parameters.

10. Sadana et al. (6,222,253 B1) is cited as substantially equivalent to Sadana et al. (643), for purposes of the rejection, except that it only discusses the two-step ion implantation sequences, with analogous subsequent annealing steps, rather than also discussing the option multiple lower temperature & dose oxygen ion implantations subsequent to the initial oxygen ion implantation (summary, especially col. 2, lines 49-col. 3, lines 7; & col. 4, line 10-col. 5, lines 37). However it is particularly noted that Sadana et al. (253) substantiates the above arguments of including "vacancies" as types of defects created in the initial oxygen ion implantation step, since in col. 4, lines 40-49 oxygen ion implantations in doses of $(3-5)10^{17}$ ion/cm² are explicitly taught to cause "Si damage clusters of Si atoms, Si in interstitial locations and Si vacancies with and/or without oxygen".

Roitman et al. (6204546 B1: abstract; summary; col. 2, lines 44-col. 4, lines 24) has substantially equivalent disclosure to Sadana et al. ((253) or (643)) for purposes of the rejection, except is more similar to (253) & teaches at the first ion implantation creates "silicon crystal and defect regions having stacking faults and dislocation defects" (col. 2, lines 56-57), where dislocation is considered to be substantially equivalent to vacancies, and discusses buried oxide layer thicknesses in the range of 300-800 Angstroms (i.e. 30-80 nm).

11. Claims 1 & 12-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Norcott et al. (6,486,037 B2, which is the child of PN 5,930,643 to Sadana et al & contains essentially the same teachings with respect to the claims as written).

The applied reference has a common assignee & overlapping, but not identical inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claims 1 & 12-22 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-39 of U.S. Patent No. 6,486,037 B2 (Norcott et al.), as discussed above & with respect to its parent Sadana et al. (5,930,643). Although the conflicting claims are not identical, they are not patentably distinct from each other because the varying semantics, different orders of claiming limitations & overlapping ranges create obvious variations on a theme, where the more specific independent claim limitations of the patent are encompassed by the more generic present application's limitations, such as those in Norcott et al. directed to multiple oxygen ion implantation steps whose initial step produces buried defects which are considered to encompass vacancies. Norcott et al.'s

initially more generic oxidizing step is further defined in their dependent claims to affect annealing with parameters and gases as claimed.

12. Claims 1-25 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-38 of copending Application No. 10/674,648, optionally in view of Houston et al. (2002/0086463 A1), or Sadana et al. (643).

Although the conflicting claims are not identical, they are not patentably distinct from each other because the two applications contain process limitations directed to the same or analogous steps with overlapping ranges, claimed in different orders to produce variations in scope, and employing varied nomenclature to effect semantics or scope differences. For instance the (647) application starts with "providing a graded porous Si-containing structure", while the present case is providing "a structure comprising at least a Si-containing substrate that has a region of vacancies or voids located therein", where it is noted that voids can be considered equivalently to porosity & in both these cases n-type or p-type dopants are employed & like electrolytic anodization process preformed in association with the providing step, which according to the (648) specification ([0047-53]) is what produces the graded porous microstructure within the Si-containing substrate /structure, noting that the present applications' claims encompass the more specific porous limitation of (648), where the phrasing may or may not mean that the porosity is graded, however having a region of voids implies also having regions without voids, thus areas of greater and lesser porosity, i.e. a type of grading. Hence, these limitations when considered with their dependent claims concerning providing steps are seen to be equivalent and/or significantly overlapping. Similarly the (648) dependent claims concerning forming a capping layer are overlapping with this (647) application's dependent claims of forming a [single crystal] silicon-containing layer (112 problems). The various annealing, "pre-oxidation", "post oxidation", ion implanting & oxidizing steps in the (648) dependent claims of the copending application are of overlapping scope with the bake step,

implanting step, annealing of the present application (647). Thus the claims of these two applications may be considered obvious variations on a theme with highly overlapping scope.

It is noted that the present application has specific limitations to implanting oxygen ions & annealing the ion implanted structure in the independent claims, which is encompassed by the copending (648) applications oxidizing step (+steps called pre-& post oxidation), which may be further described by various atmospheric and temperature parameters affecting oxidation, as well as affected by implantation of ions, called "neutral ions", whose meaning is unclear, but not really neutral as defined & may be implanted at any time during the process, thus inclusive as part of the oxidation process, but oxygen ion implantation is not explicitly claimed as a possible oxidation process in the (648) application. Given oxygen ambience & oxygen gas for oxidizing & as well as possible ion implantation in the (648) claims, it would've been obvious to one of ordinary skill in the art to supply that oxygen ambient via oxygen ions from oxygen gas to implant as claimed in the present (647) claims, or alternately with respect to particular parameters, there is considerable overlap & furthermore they would have been expected to be determined & optimize via the routine experimentation dependent on the particular silicon-containing materials employed, as well as desired depths & thicknesses of buried oxide layers being produced. Optionally, either Houston et al. or Sadana et al., both discussed above, provide teachings concerning the known use of employing oxygen ion implantation in the oxidizing process of creating buried oxide layers in combination with oxygen annealing techniques, hence it would've been further obvious to one of ordinary skill in the art to employ such known processes for providing the details of creating the desired buried oxide layers, which would have been expected to be effective for reasons as discussed above.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

13. Claims 1-25 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 14-18 of copending Application No. 11/164,632 (Chidambarrao et al., 2007/0122956 A1), in view of Sadana et al. (643) discussed above in sections 7-9.

The application to Chidambarrao et al. claims creating discrete porous semiconductor regions below the surface of an active semiconductor region, where the porous region is oxidized, and where the porous semiconductor is formed via implanting p-type dopant into a silicon region, then HF electrolytically anodizing, followed by a hydrogen bake & deposition of an epitaxial layer of semiconductor over the implanted region. The claims of Chidambarrao et al. are narrower in that they are directed to formation of a specific device, a field effect transistor (TFT), but broader in that they do not claim any specific parameters for the porosity formation or hydrogen bake or oxide layer thickness, or specific techniques for the oxidizing, including parameters therefore, however Sadana et al. (643) provide specific oxidizing procedures as claimed for creating buried oxide layers consistent with the process claimed by Chidambarrao et al., such that one of ordinary skill in the art would have founded it obvious to accomplish the claimed generic oxidation step of Chidambarrao et al. via a procedures via oxygen ion implantation & annealing sequences as set forth in Sadana et al. (643), with expectation of effectively creating buried oxide layers, with effective means of controlling thickness, such as to the exemplified 1000 Angstroms, i.e. 100 nm, since like materials are being employed, including the possible presence of an intervening surface layer. While Chidambarrao et al. do not claim a particular thickness for the buried oxide layer, it would've been obvious to one of ordinary skill in the art to control that thickness via techniques such as discussed in Sadana et al., so as to provide known useful thicknesses for TFT structures, which would've been expected to be inclusive of thicknesses as claimed. With respect to specific parameters for the electrolytic anodization process & H-bake, it would've been obvious to one of ordinary skill in the art to performed routine experimentation in order to optimize this processing procedures for specific the specific semiconductor materials & enduses of the buried oxide layer.

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This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marianne L. Padgett whose telephone number is (571) 272-1425. The examiner can normally be reached on M-F from about 8:30 a.m. to 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks, can be reached at (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MARIANNE PADGETT
PRIMARY EXAMINER